appears to be misreading the Nakatsuka reference. In particular, the office action states "thus, when Nakatsuka discloses converting a "picture logical address" into "a physical address" to access the graphics processor (see column 9, lines 47-50), it can be seen that the "picture logical address" previously translated from the "logical address" by the data processor to access pixel data is further translated by the graphics processor to access matrix data." However, a fundamental error appears to be made in that the Nakatsuka reference does not teach that the data processor uses the "previously translated" picture logical address referred to in column 9, lines 5-8. In fact, as Applicant has attempted to point out in the previous response, these two sections that the office action alleges talk about the same embodiment, in fact refer to two different embodiments. For example, the teachings in column 9, lines 5-8 refer to one embodiment whereas the teachings in column 9, lines 47-50 refer to a different embodiment. As such, there is no previous translation of the picture logical address by the data processor as alleged in the office action. To the contrary, the cited reference states the opposite.

For example, the cited reference specifically states "while in the foregoing description, access to picture data has been explained, and a case where the calculation of a matrix is carried out by the data processor 120, it is possible to directly effect access in a way similar to the operation in the above graphics processor unit 120 by storing the matrix data in the memory unit 200 as a physical address in the form of a tile type address...like the pixel data." (column 9, lines 40-48). As such, a portion of the reference cited by the Examiner to support that a previous translation has been made in fact states the opposite. The cited portion of the reference specifically states that no translation is necessary by the data processor since the data processor already stores the matrix data as a physical address which does not need to be converted. This is

done in such a way as in the previous embodiment where the graphics processor stored information like the pixel data in memory so it would not need to perform a translation.

In fact, it does not appear that it would make sense to perform a further translation since only one translation is necessary by the graphics processor. Since column 9, lines 40-60 refer to the embodiment where the data processor stores matrix data as a physical address in memory there is no translation performed by the data processor. When the graphics processor wishes to access the data however, it must perform a single translation "for converting the picture logical address into a physical address in order to effect access to the matrix data by the graphics processor 120." As such, Applicant respectfully submits that these claims are in condition for allowance.

Applicant also respectfully reassert the relevant remarks made in the previous office action with respect to the other claims as the same rejection has been maintained as to those claims.

Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: 7-7-04

By: Christopher J. Reckamp
Christopher J. Reckamp
Registration No. 34,414

Vedder, Price, Kaufman & Kammholz, P.C.
222 N. LaSalle Street
Chicago, Illinois 60601
PHONE: (312) 609-7599
FAX: (312) 609-5005